

Optimizing the Power Integrity Ecosystem

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2020.3.12

Keysight Power Integrity Applications Expert



How to Design for Power Integrity

5 Part Series

1

How to Design for Power Integrity:
Finding Power Delivery Noise Problems



Steven Sandler
Founder
PICOTEST
Author of
Power Integrity
A McGraw-Hill
publication.



Keysight EEsof EDA
"How to" Video



2

How to Design for Power Integrity:
Selecting a VRM



Steven Sandler
Founder
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A McGraw-Hill
publication.

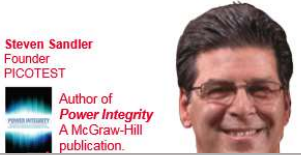


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3

How to Design for Power Integrity:
Measuring, Modeling, Simulating
Capacitors and Inductors



Steven Sandler
Founder
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4

How to Design for Power Integrity:
DC-DC Converter Modeling and Simulation



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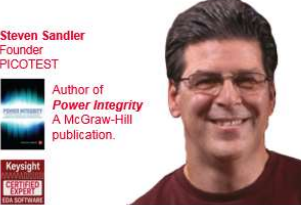


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5

How to Design for Power Integrity:
Optimizing Decoupling Capacitors



Steven Sandler
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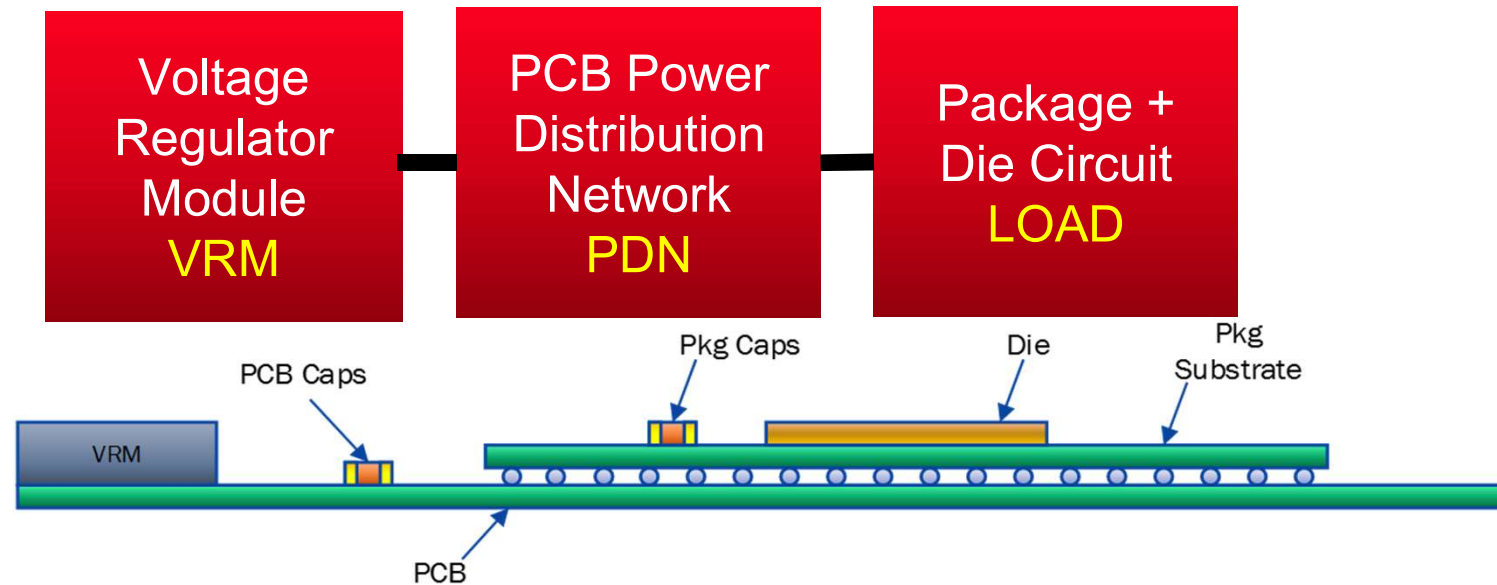
.... More coming

3 Step Decoupling Capacitor Optimization

Design Methodology for DeCap Optimization

1. Calculate 1st order approximations using simple resistor, inductor, capacitor **R-L-C** models
-  2. Use **Target Z** to optimize the decoupling capacitor selection using high fidelity EM models (**ADS PIPro**)
3. Validate with full **Power Integrity Eco-System** simulation in ADS

Power Integrity Target Impedance



Target Impedance Calculation

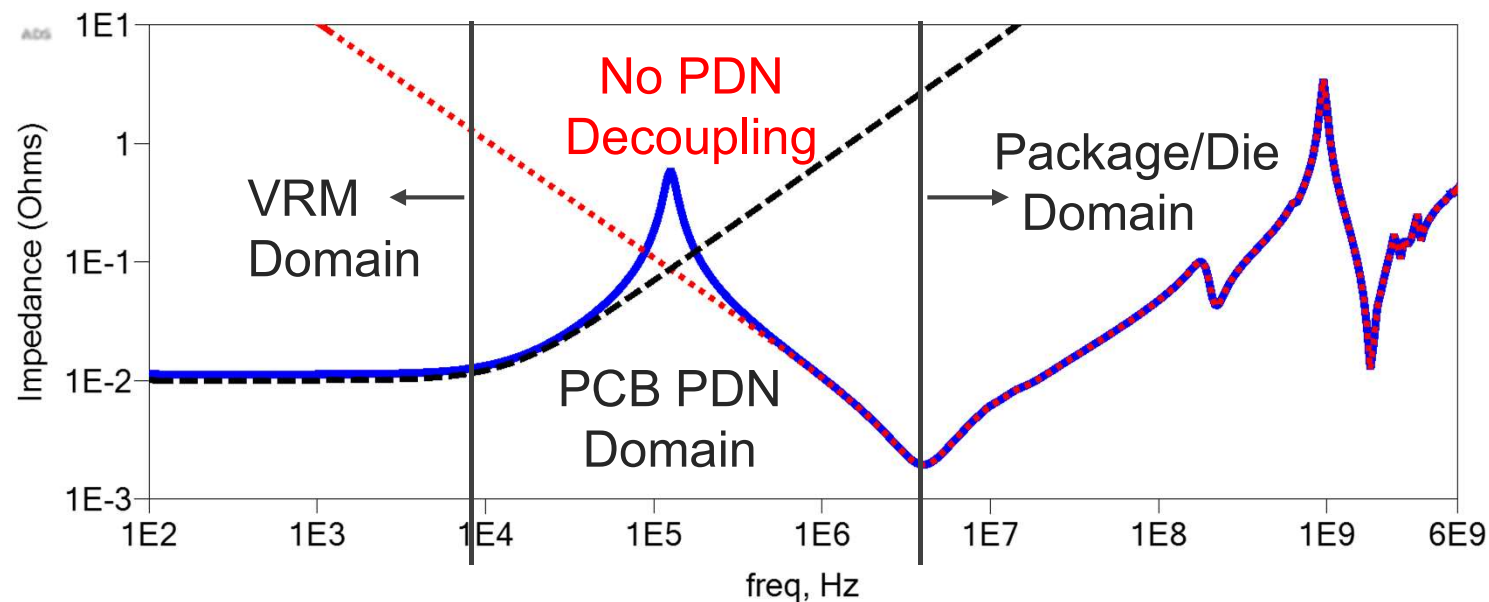
$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$

PDN Impedance Mask Maximum Frequency

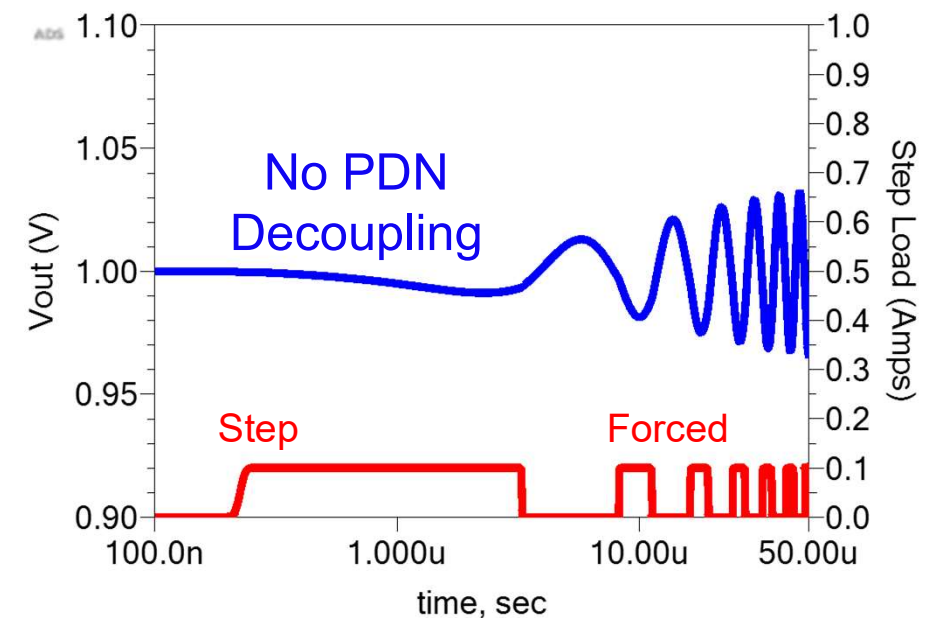
Package/Die S-parameter Estimates Max L:

$$\text{Max } L_{PDN} = C_{pkg} * Z_{Target}^2$$

**Frequency Domain
Impedance at the Package Pin**



**Time Domain
Voltage and Current vs. Time**

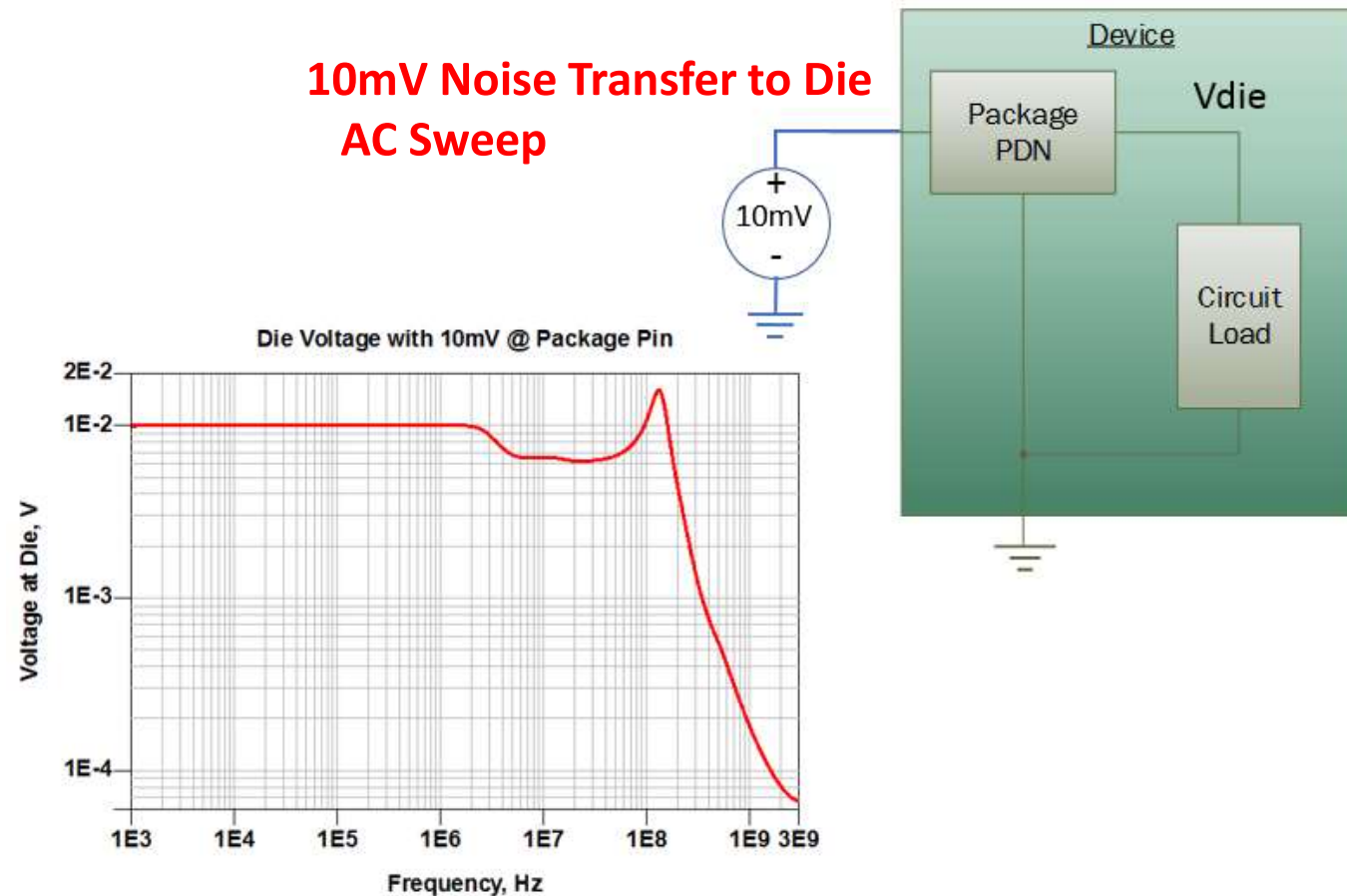


Flat C Decoupling

$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2} \quad C_{decap} = \frac{ESL_{Cbulk}}{Z_{Target}^2}$$

Package/Die S-parameter Blocks Block High Frequencies

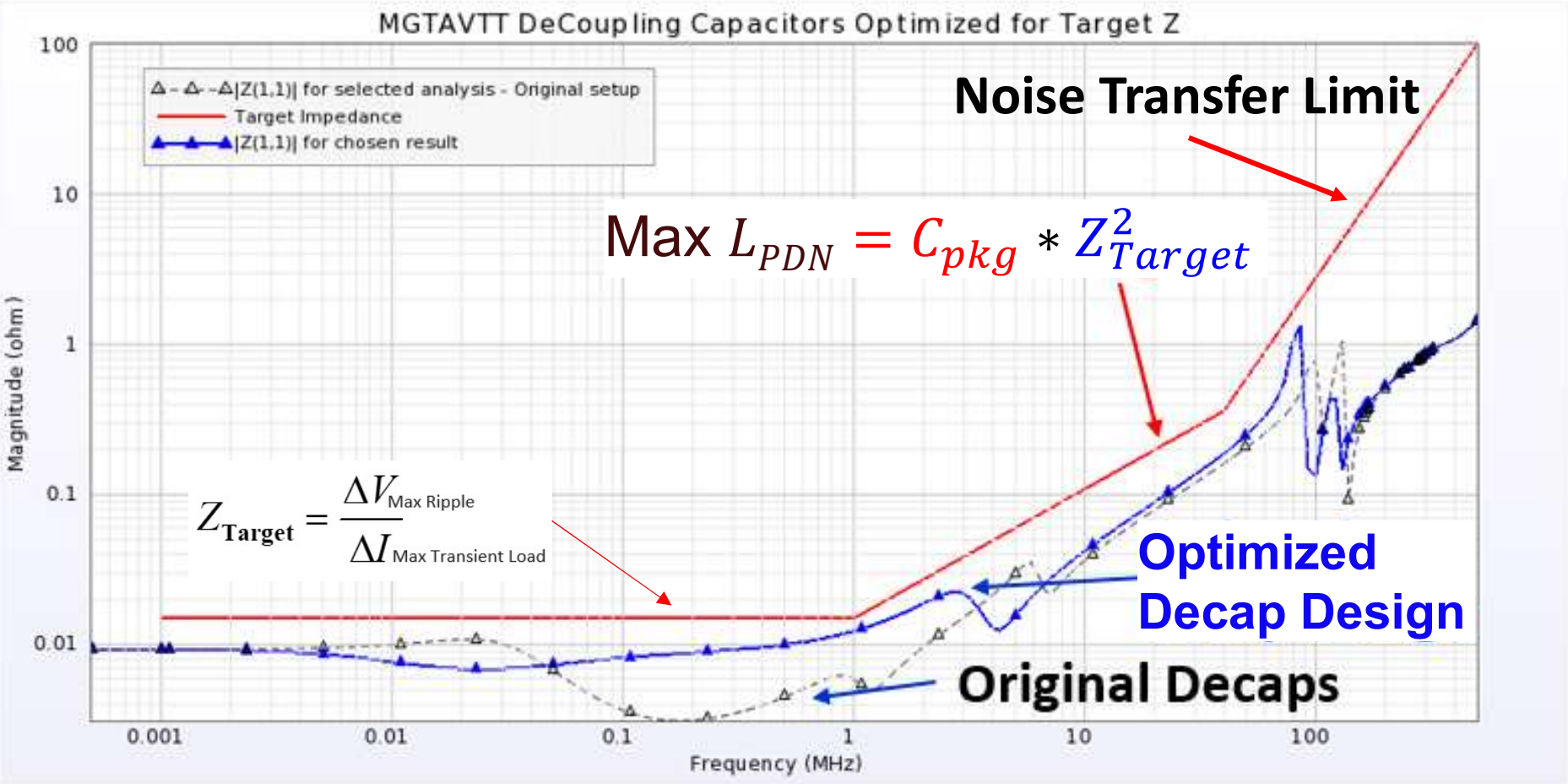
Noise transfer to the die is 1 to 1 at low frequencies but is attenuated at high frequencies.



Optimize Decoupling for Max Performance/Cost Ratio

Target Z Decoupling Capacitor Optimization

40% Reduction
in Part Count



Capacitors

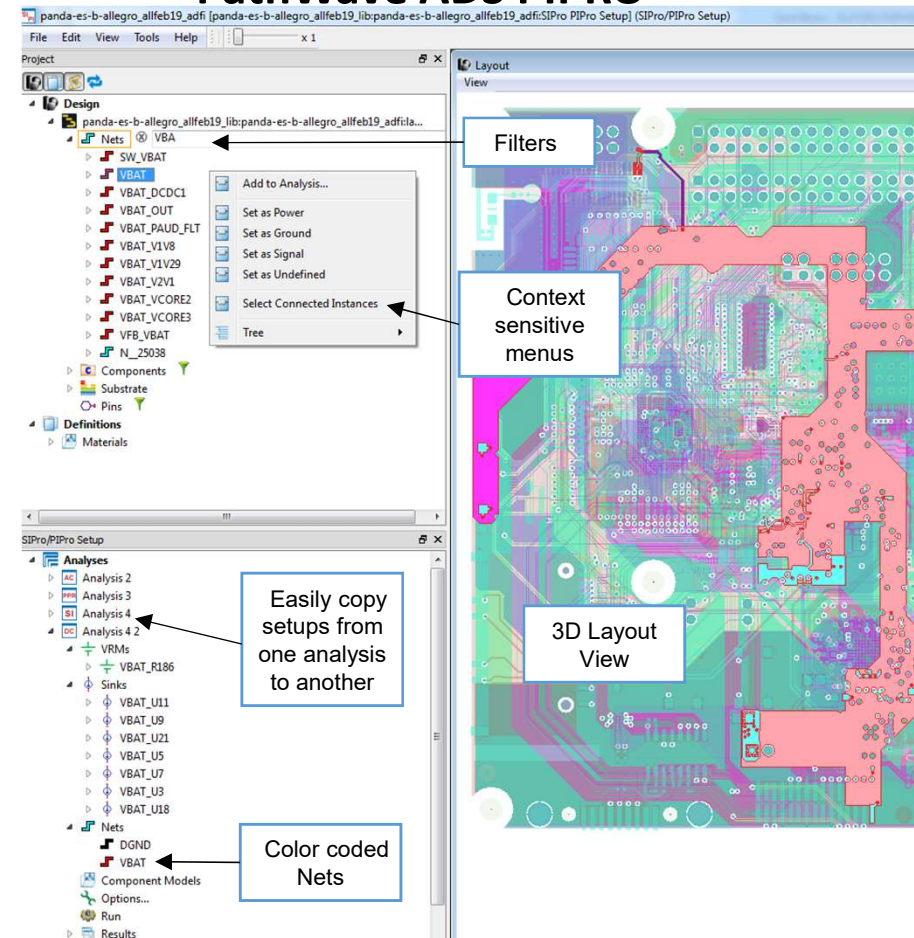
Yes	C190	330 uF
Yes	C215	330 uF
Yes	C216	330 uF
Yes	C218	330 uF
Yes	C303	220 nF
Yes	C305	220 nF
Yes	C750	220 nF
Yes	C753	220 nF
Yes	C757	220 nF
No	C217	100 uF
No	C225	100 uF
No	C315	4.7 uF
No	C316	4.7 uF
No	C778	4.7 uF
No	C779	4.7 uF
No	C780	4.7 uF

Net Based EM Tools Make it Easy

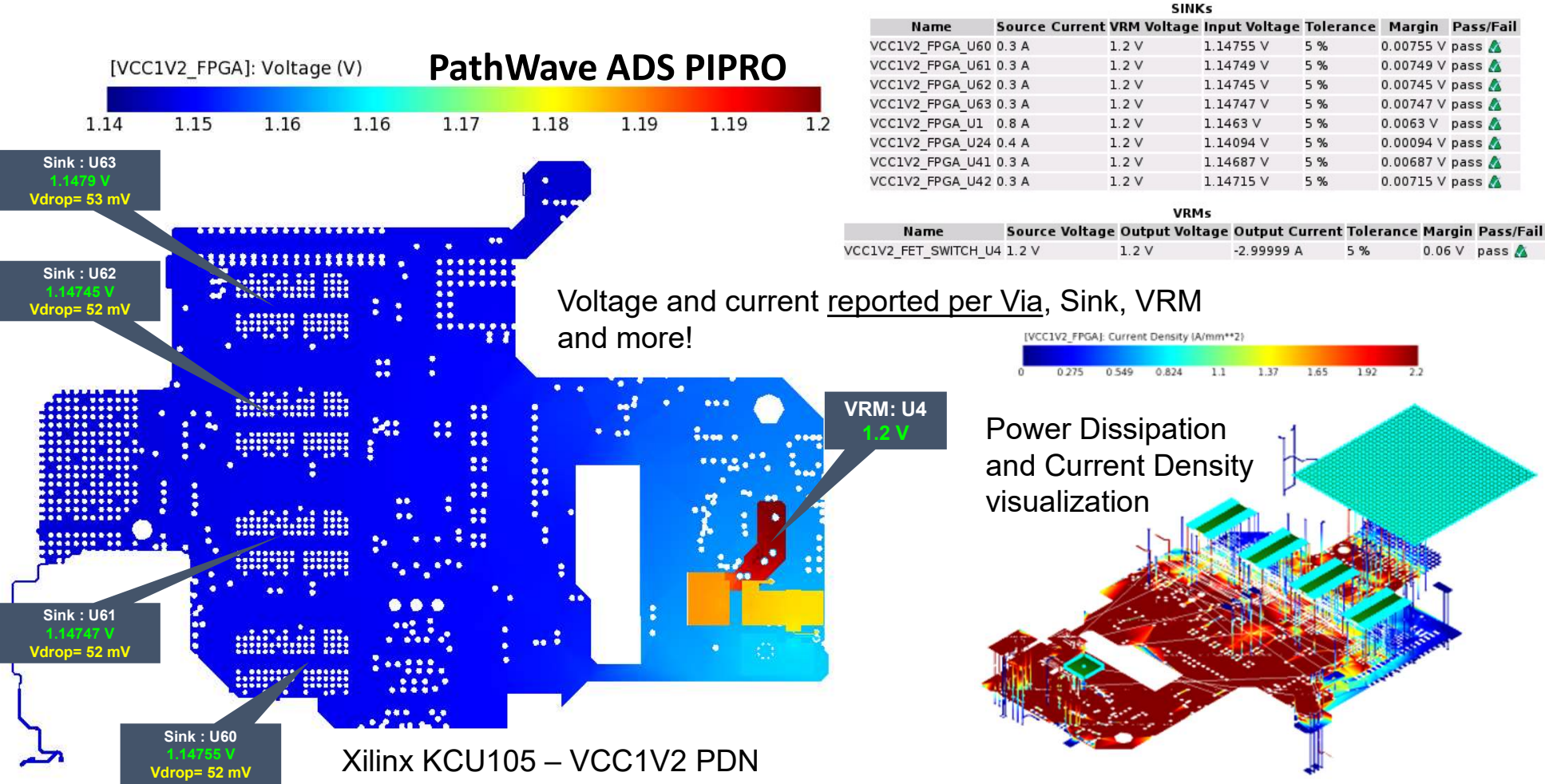
Designed for Usability

- Filter by Net
- Filter by Component
- Right-click to add-to-analysis
- Drag & Drop
- Hierarchical search for complex selections
- Context sensitive menus e.g. *'Select instances connected to ONLY the selected nets'*

PathWave ADS PIPRO

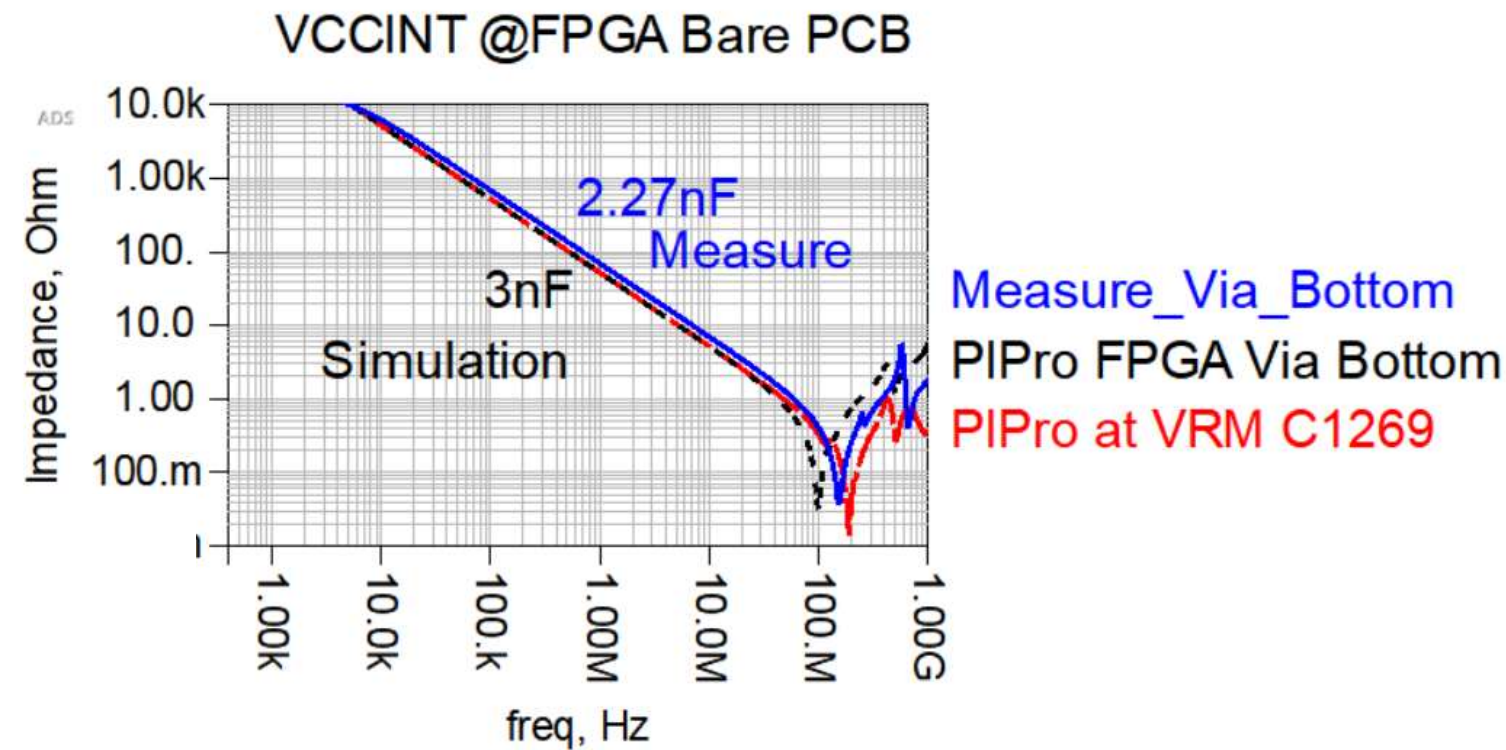
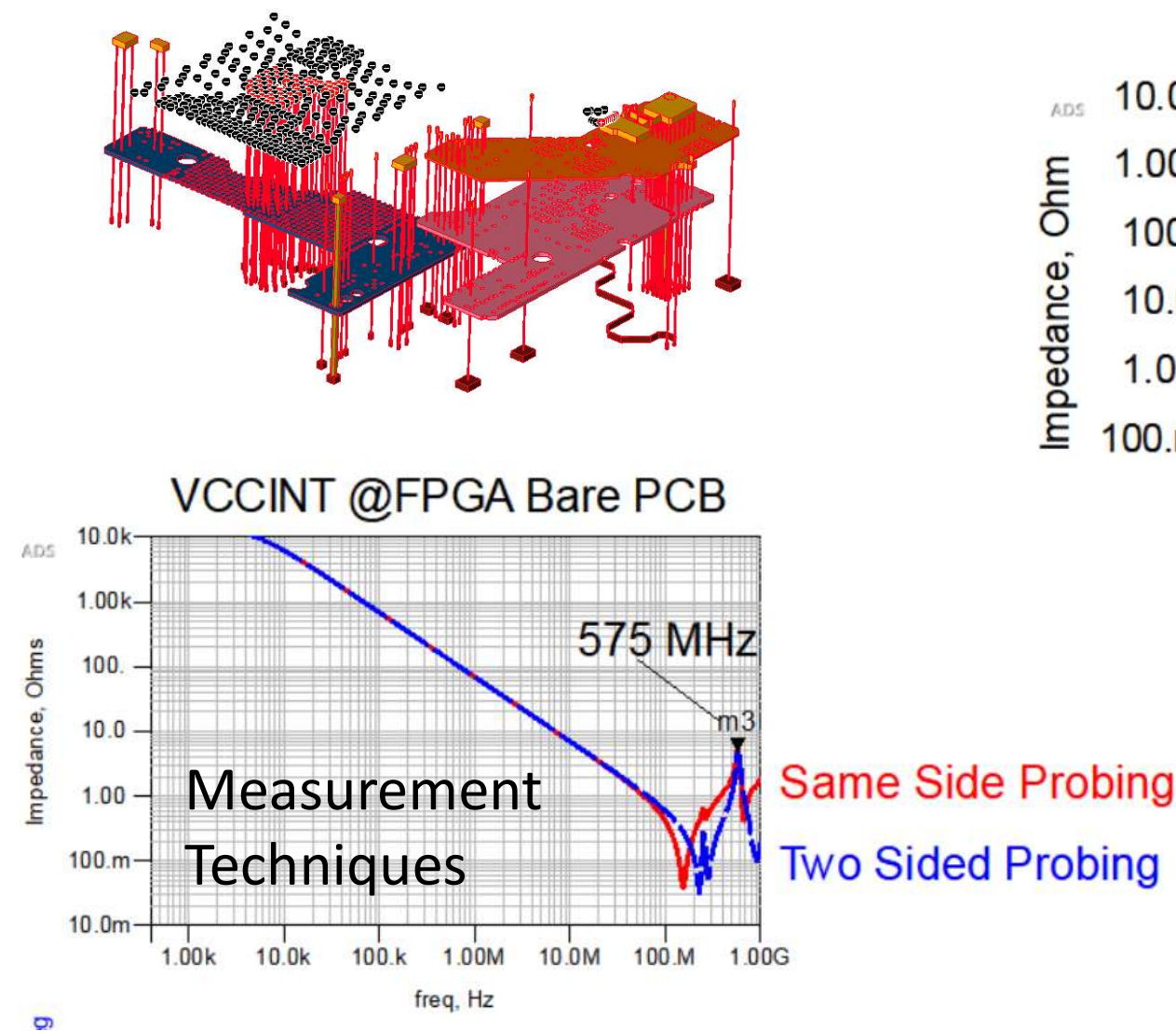


Always Start with DC IR Drop!



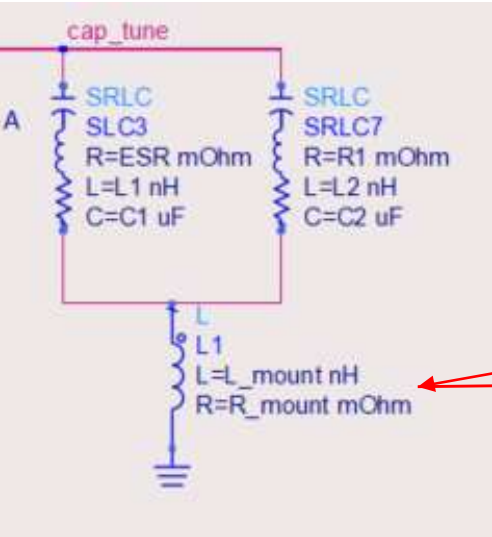
PCB PDN Model

Simulation vs. Measurement

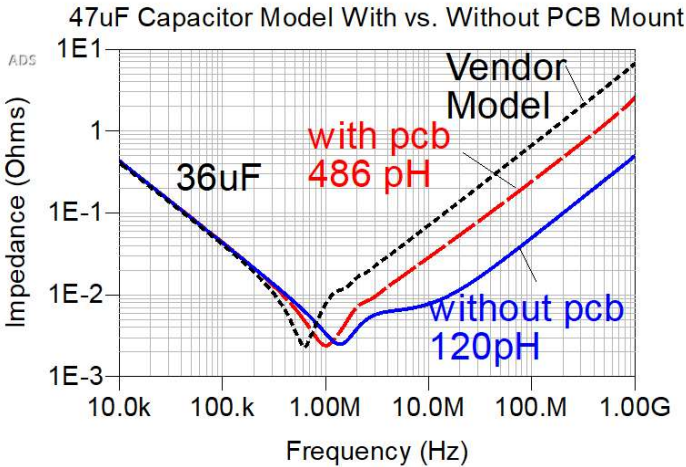
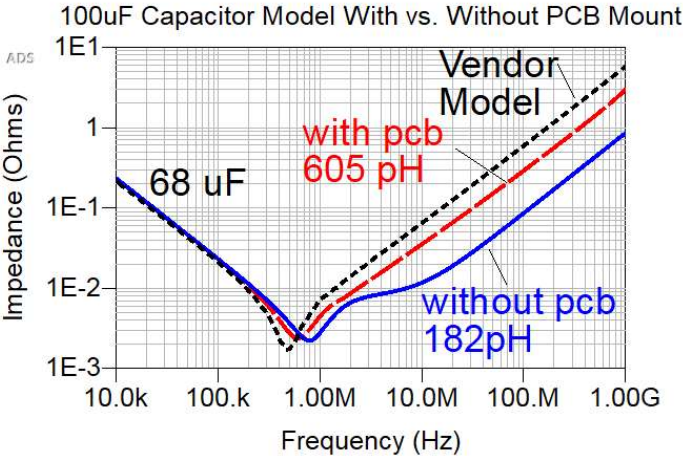
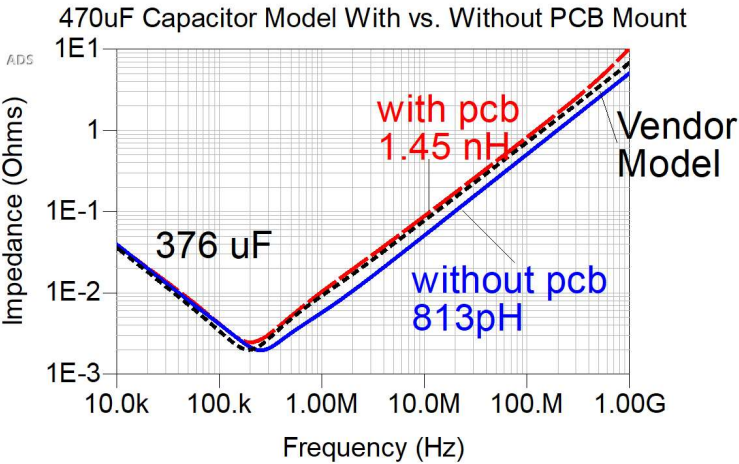
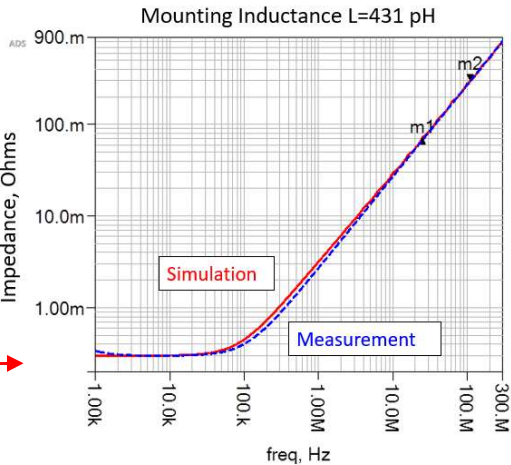


Capacitor Models without Mounting Inductance

S11



PCB EM Model
includes this...
remove from
capacitor model.

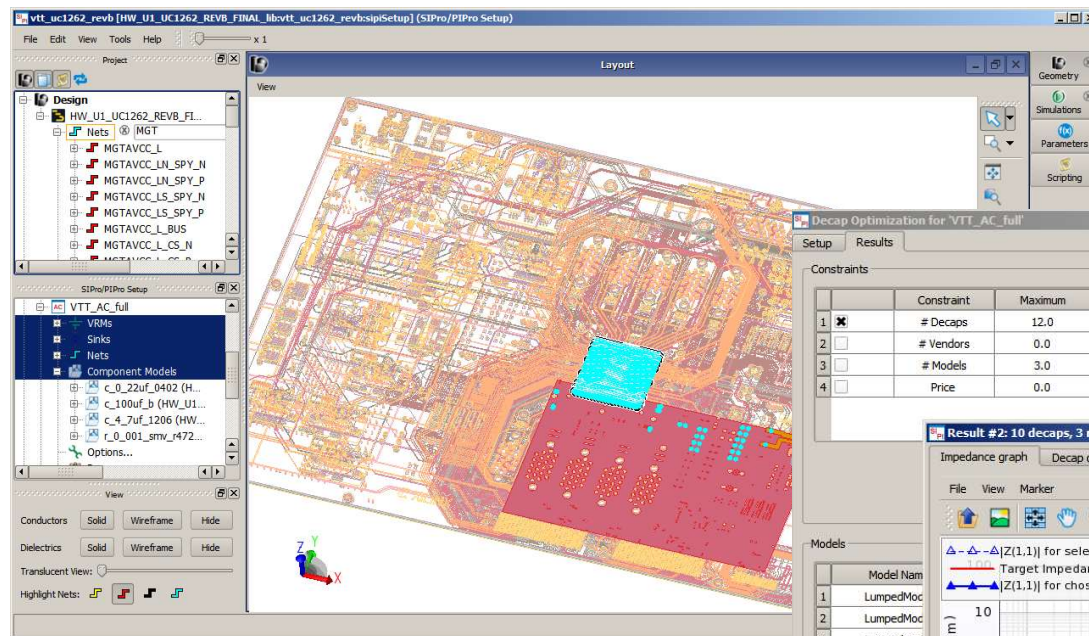


PathWave ADS PIPro EM Simulation of the PCB PDN

Easy setup for high port count simulations

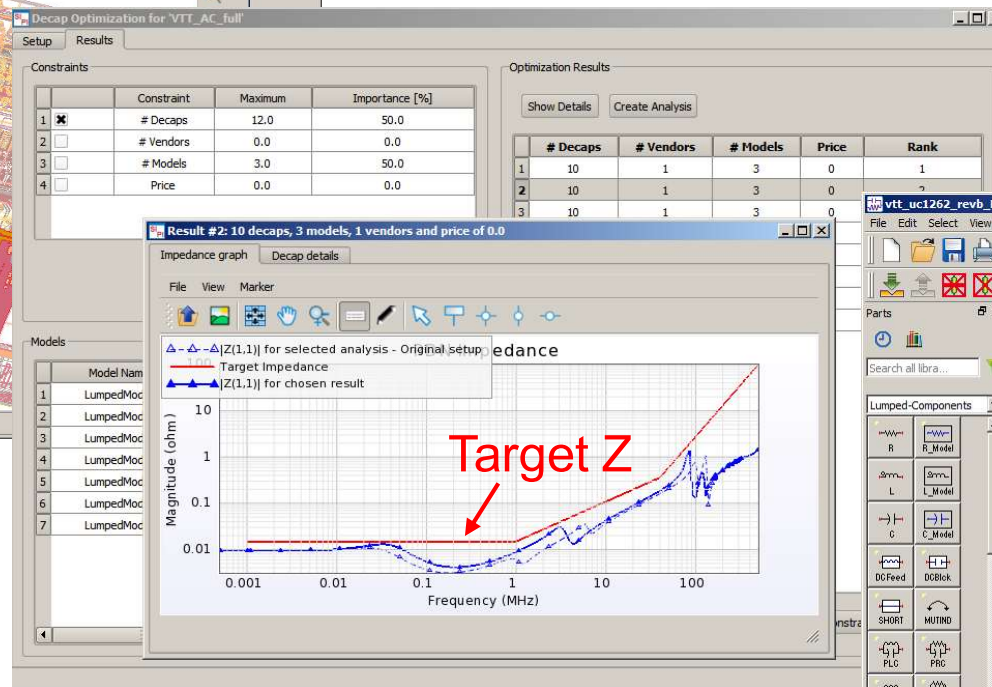
1) IMPORT THE PCB

- Select VRM, Sink, Nets, Components
- Run EM AC Frequency Sweep



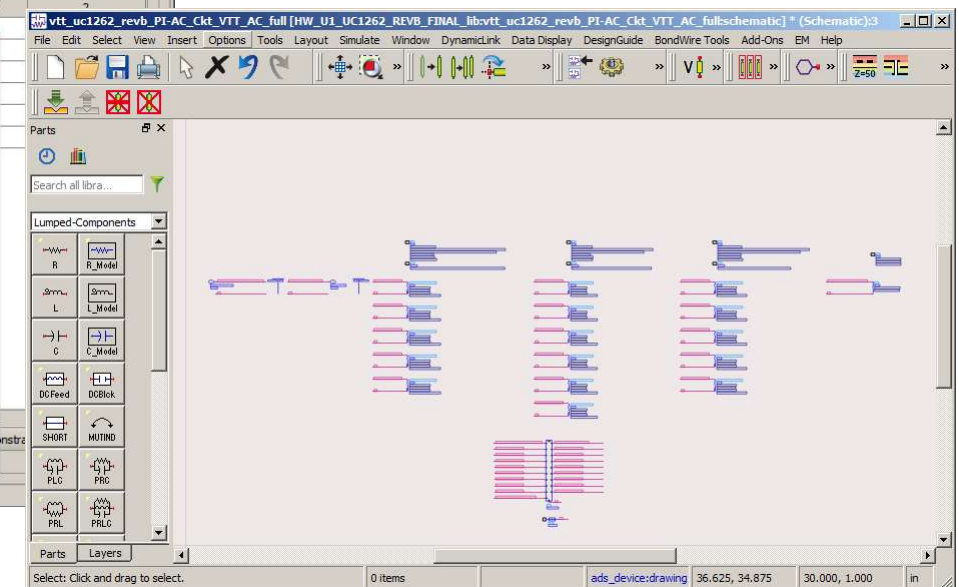
2) OPTIMIZE DECOUPLING

- Select capacitor models
- Setup optimization goals
- Run Optimization



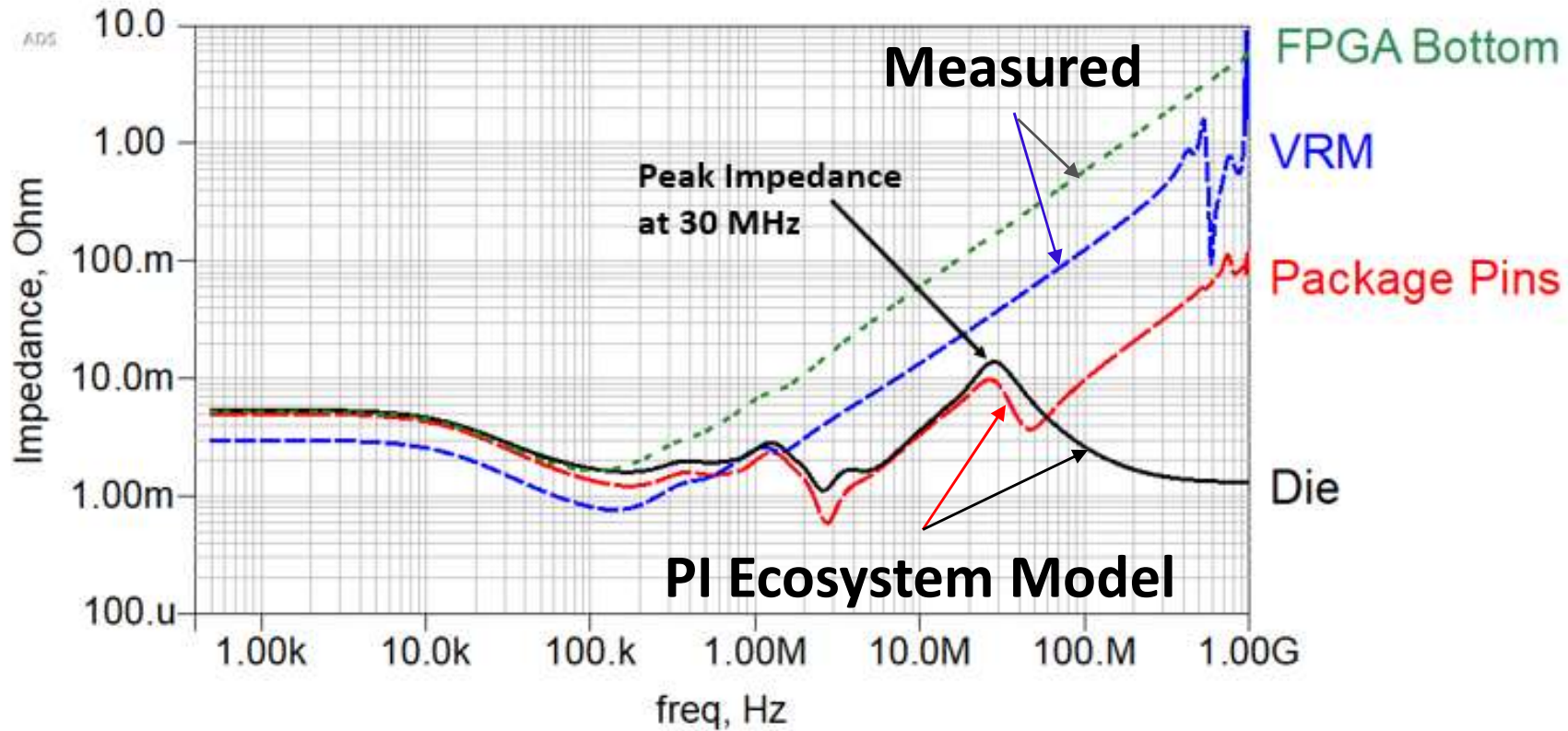
2) GENERATE SCHEMATIC

- Auto generate schematic with PCB PDN EM model and optimized capacitors.



Simulated PI Ecosystem Impedance is Easier than Measurement

Impedance measurements did not see the resonance at 30 MHz!



- Decoupling capacitors dominate the impedance of the VCCINT PDN.
- Measurements with VCCINT are only accessible on the bottom side of the FPGA and include the via inductance.
- PIPro PDN EM model with package/die (CPM) in ADS schematic accurately predicts impedance peak that measurement could not see.

3 Step Decoupling Capacitor Optimization

Design Methodology for DeCap Optimization

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3. Validate with full **Power Integrity Eco-System** simulation in ADS

Voltage Regulator State Spaced Averaged Models

Measurement Based VRM Modeling

Steve Sandler – PICOTEST



4

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Measured Output Z
Power OFF and Power ON

Capacitor RLC Model
Measure Based Optimization

Measured Capacitor Impedance

Measured Power Supply Rejection Ratio

Large Signal Output
Switching Ripple Transients

PDN Decoupling and Load

IMPEDANCE

LOAD

IMPEDANCE

Variables

Simulation Controllers

Tuned Variables for Matching
VRM Model with Measurement

Three Separate Simulations in one Schematic

Modeling the Power Integrity Ecosystem

$$\text{VRM} + \text{PDN} + \text{Load} = \text{PI Ecosystem}$$

Three Separate Simulations in one Schematic

Simulation Controllers

**AC**
AC
AC1
Start=100 Hz
Stop=40 MHz
Step=

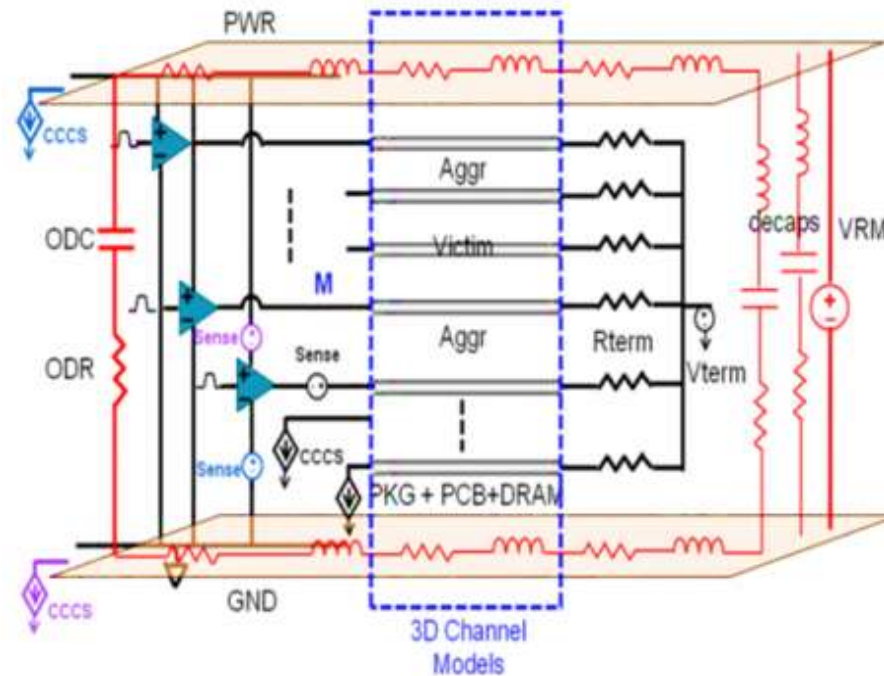
**S-PARAMETERS**
S_Param
SP1
Start=100 Hz
Stop=40 MHz
Step=

**HARMONIC BALANCE**
HarmonicBalance
HB1
Freq[1]=Fs
Order[1]=256

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SI and PI Co-EM Simulation



Power and Signal Nets
in the same EM
simulation

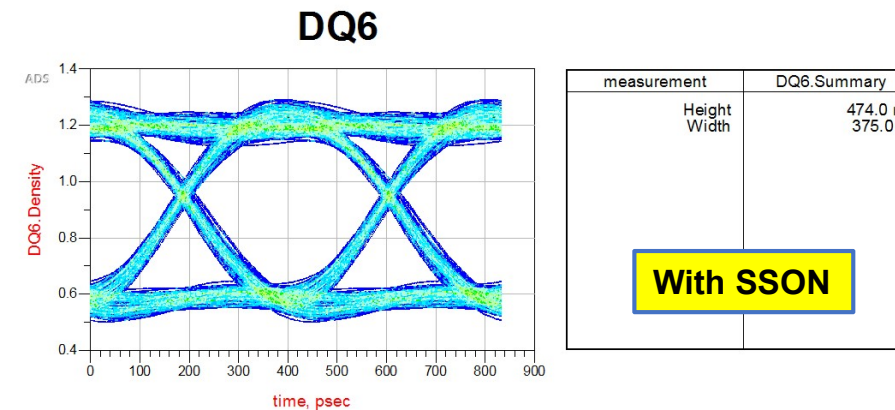
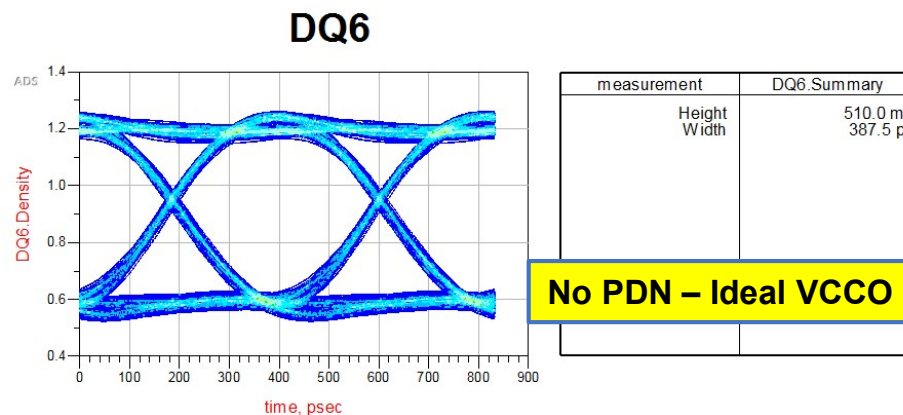
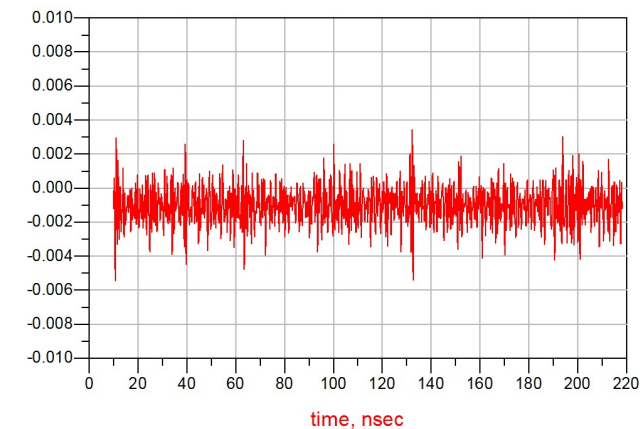
- Xilinx Kintex FPGA and Micron DDR4 IBIS models



Simultaneous Switching Noise (SSN)

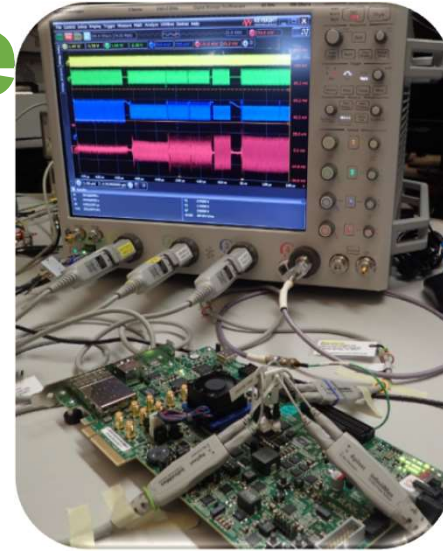
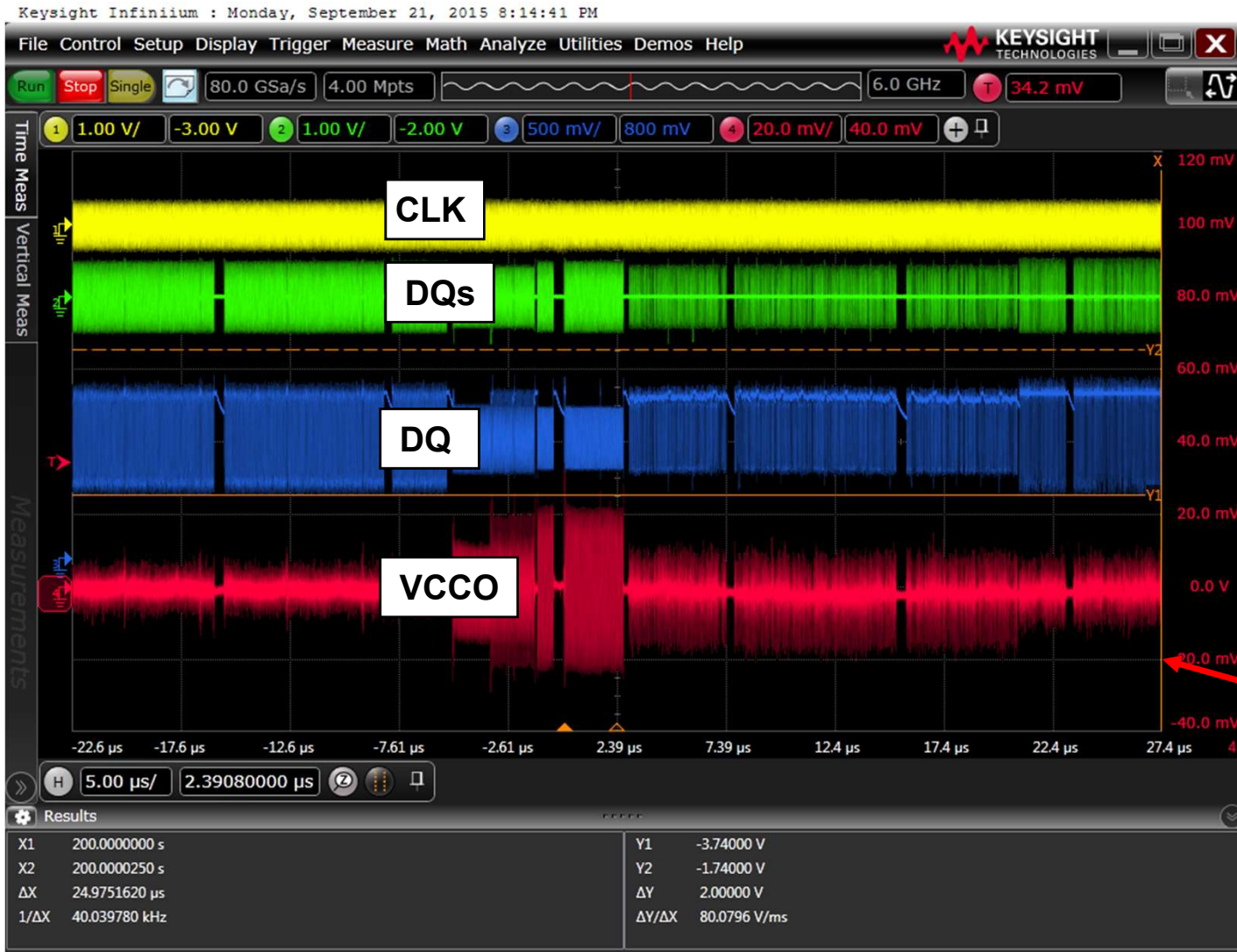
- Shows SSN noise voltage at VCCO pin, which is similar to the measured data
 - Both eye width and height are reduced by SSO noise, as expected.
 - 387.5p → 375p, 510mV → 474mV respectively

VCCO Pin Noise Voltage By SSN



SSO Noise Measured Example

- Simultaneous Switching Output Noise (SSON)



Summary

- How parallel resonances lead to significant voltage ringing on the power rail
- How to calculate decoupling C for a flat target Z
- The impact of Capacitor PCB mounting parasitics
- ADS with PIPro DeCap Optimization for reduced part count and full PI Ecosystem simulation

PDN Disasters Do Exist – Always Look at the PDN Impedance!

Video #1

1

How to Design for Power Integrity:
Finding Power Delivery Noise Problems

 Keysight EEsaf EDA
"How to" Video

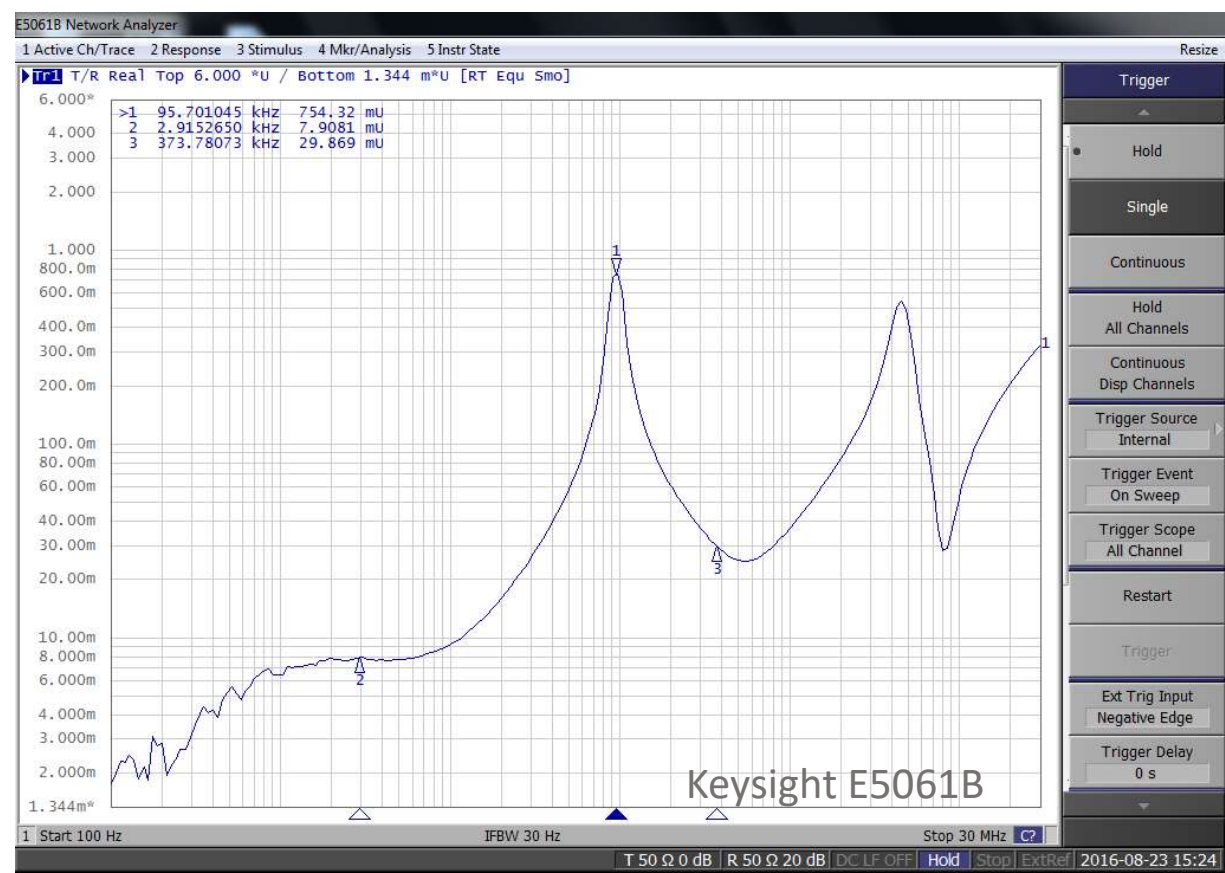
Steven Sandler
Founder
PICOTEST



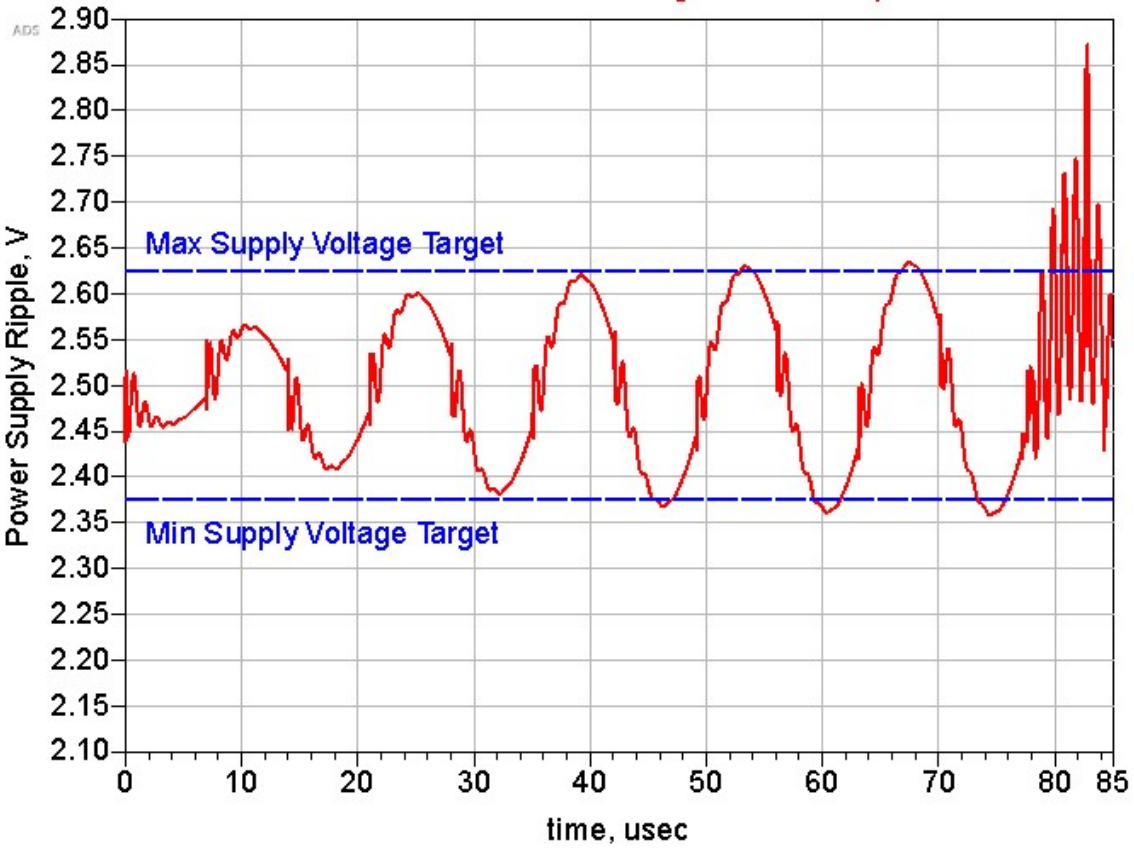
Author of
Power Integrity
A McGraw-Hill
publication.



Frequency Domain Shows Resonances



Time Domain Excitation – Rogue Wave Failure



Hands-On Lab:

200128_ADS_PI_Lab4_DeCap_Optimize_wrk.7zads

Basics – Instructor Led Demo

Flat Z Capacitor Selection – 1st Order Approximations

Explore –

Parallel Capacitor Lumped SPICE vs. Distributed EM Models

Advanced –

Advanced - PIPRO Decoupling Capacitor Optimization DDR4 DIMM

Power Integrity Workshop Summary

Step 1: Rules of Thumb for Flat Z Design starting with a Target Z

Step 2: EM Model of the PCB + Decap Optimization

Step 3: Eco-System with VRM model, PCB PDN, and Load

Step 4: Measure/V&C

Contact us with your questions: steve@picotest.com heidi_barnes@keysight.com jackc@xilinx.com



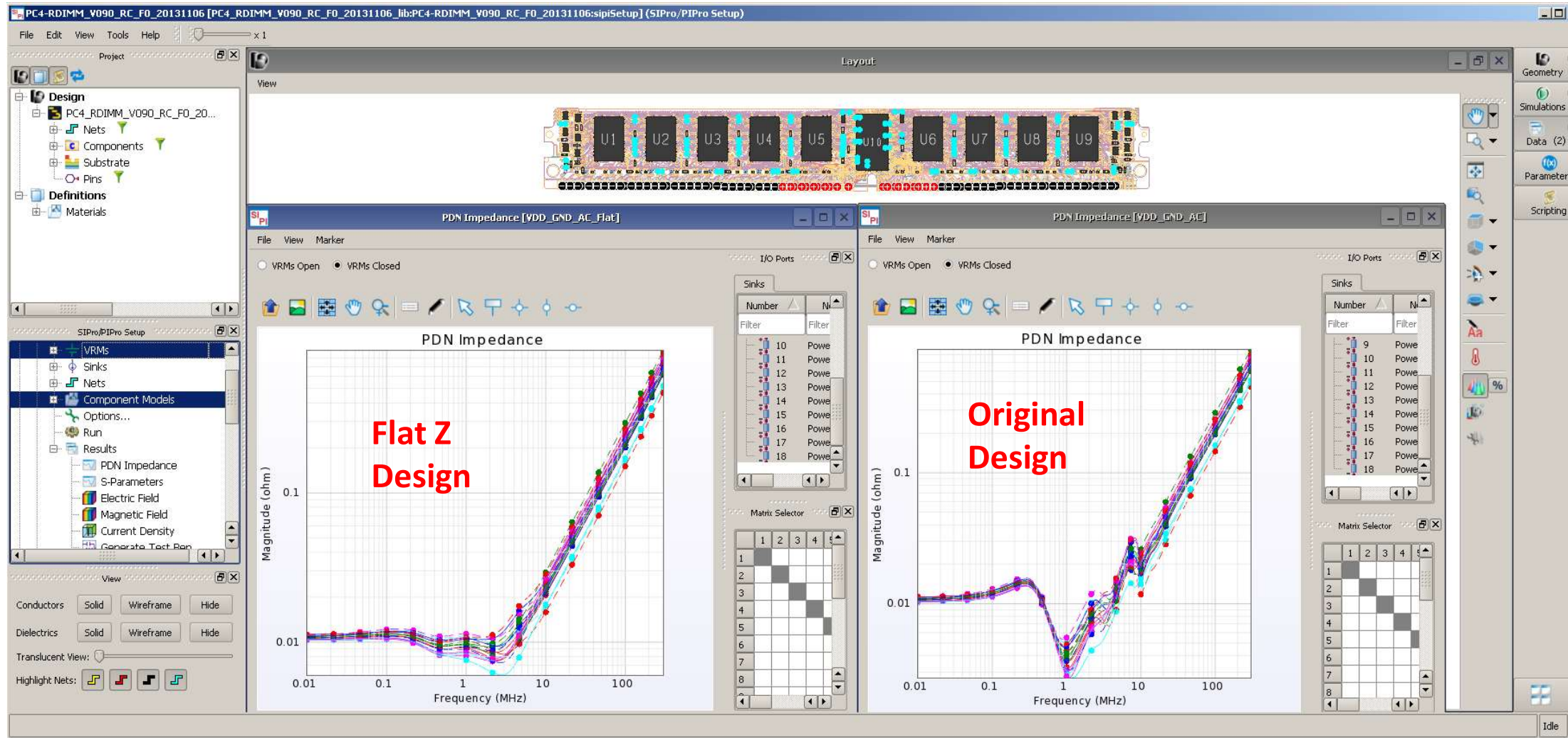
PathWave ADS with PIPro

*“....the only tool that can do end to end simulation of the power integrity ecosystem”
Steve Sandler, Picotest.com*

PCB Decoupling Capacitor Optimization

Flat impedance vs frequency for best performance

Flat Z with 40% fewer capacitors



Result #2: 25 decaps, 3 models, ...

Impedance on	Decap details
Enabled	Name
Yes	C104
Yes	C106
Yes	C107
Yes	C108
Yes	C109
Yes	C110
Yes	C111
Yes	C116
Yes	C119
Yes	C120
Yes	C123
Yes	C24
Yes	C31
Yes	C33
Yes	C35
Yes	C37
Yes	C42
Yes	C44
Yes	C46
Yes	C54
Yes	C95
Yes	C96
Yes	C97
No	C100
No	C102
No	C105
No	C60
No	C63
No	C66
No	C68
No	C70
No	C75
No	C76
No	C77
No	C78
No	C81
No	C83
No	C85
No	C87
No	C91

DDR4 DIMM Example – Ships with ADS

Decoupling capacitor optimization for Flat z

